AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of the claims in the application.

Listing of Claims:

1. (Currently amended) A manufacturing method of a semiconductor integrated circuit device having a plurality of first MISFETs in a first region of a semiconductor substrate and a plurality of second MISFETs in a second region of said semiconductor substrate, comprising the steps of:

(a) forming a plurality of first insulating film portions in each of ~~between two adjacent regions of said~~ first MISFET forming regions in said first region and said second MISFET forming regions in said second region,

(b) forming a plurality of second insulating film portions over a surface of said semiconductor substrate between ~~said~~ first insulating ~~films~~film portions in each of said first and second regions,

(c) depositing [[a]] third insulating film portions over at least said second insulating film portions and said first insulating film portions,

(d) forming [[a]] first conductive film portions over said third insulating film portions in said second region,

(e) forming, after removal of portions of said third and second insulating films from said first region, [[a]] fourth insulating film portions over the surface of said semiconductor substrate in said first region, [[and]]

(f) forming [[a]] second conductive film portions over said fourth insulating film portions,

(g) forming a fifth insulating film covering said semiconductor substrate, and

(h) forming a plurality of first interconnects over said fifth insulating film

~~(g) wherein said third insulating film remains over said first insulating film in said second region.~~

2. (Currently amended) A manufacturing method of a semiconductor integrated circuit device according to claim 1, wherein each said first insulating film portion is an oxide film formed by thermal oxidation.

3. (Currently amended) A manufacturing method of a semiconductor integrated circuit device according to claim 1, wherein said third insulating film [[is]] portions are

formed by CVD.

4. (Currently amended) A manufacturing method of a semiconductor integrated circuit device according to claim 1, wherein an etching rate of said third insulating film portions is greater than that of said first insulating film portions.

5. (Currently amended) A manufacturing method of a semiconductor integrated circuit device according to claim 1, wherein said third insulating film [[is]] portions are thicker than said second insulating film portions.

6. (Currently amended) A manufacturing method of a semiconductor integrated circuit device according to claim 1, wherein said first and second conductive ~~films~~ film portions are each made of polysilicon.

7. (Currently amended) A manufacturing method of a semiconductor integrated circuit device according to claim 1, wherein [[the]] a third insulating film portion over ~~said~~ a first insulating film portion is formed so that end portions of said third insulating film ~~is~~ portion are

positioned on said first insulating film portion.

8. (Withdrawn) A manufacturing method of a semiconductor integrated circuit device according to claim 1, wherein said first insulating film forming step comprises forming a groove in said semiconductor substrate and forming an oxide film within said groove.

9. (Currently amended) A manufacturing method of a semiconductor integrated circuit device according to claim 1, wherein the first insulating film portions in said first region [[is]]are narrower than the first insulating film portions in said second region.

10. (Currently amended) A manufacturing method of a semiconductor integrated circuit device according to claim 1, wherein ~~said~~ a first insulating film portion in said second region is ~~also~~ formed ~~at both~~with parts underlying ends of ~~said~~ a first conductive film portion~~forming region~~.

11. (Currently amended) A manufacturing method of a semiconductor integrated circuit device according to claim 1, wherein said first insulating film ~~is also~~ portions

include portions formed at ~~both~~ ends of the ~~first conductive film~~ second MISFET forming ~~region~~ regions within said second region, and

said manufacturing method further comprises forming first semiconductor regions in the semiconductor substrate below the first insulating film ~~formed~~ portions at ~~both~~ ends of said ~~first conductive film~~ second MISFET forming ~~region~~ regions, and

forming second semiconductor regions within said first semiconductor regions but ~~outside of~~ beside the first insulating film ~~formed~~ portions at ~~both~~ the ends of ~~the first conductive film~~ said second MISFET forming ~~region~~ regions.

12. (Currently amended) A manufacturing method of a semiconductor integrated circuit device according to claim [[1]] 11, wherein the impurity concentration of said first semiconductor regions is lower than that of said second semiconductor regions.

13. (Currently amended) A manufacturing method of a semiconductor integrated circuit device having a plurality of first MISFETs in a first region of a semiconductor

substrate and a plurality of second MISFETs in a second region of said semiconductor substrate, comprising the steps of:

(a) forming a plurality of first insulating film portions in each of ~~between two adjacent regions of said~~ first MISFET forming regions in said first region and ~~said~~ second MISFET forming regions in said second region,

(b) forming a plurality of second insulating film ~~on~~ portions over a surface of the semiconductor substrate between said first insulating ~~films~~ film portions in said first and second regions,

(c) depositing [[a]] third insulating film portions over at least said second insulating film portions and said first insulating film portions,

(d) removing said third insulating film portions from said first region without removing said third insulating film over said first insulating film portions in said second region,

(e) depositing a first conductive film in said first and second regions ~~on~~ over said semiconductor substrate,

(f) removing said first conductive film from said first region and a portion of said first conductive film from said second region,

(g) forming [[a]] fourth insulating film ~~on~~ portions over the surface of said semiconductor substrate in said first region, [[and]]

(h) forming a second conductive film in said first region,

(i) forming a fifth insulating film over at least said first and second MISFET forming regions and said third insulating film portions formed over said first insulating film portions, and

(j) forming a plurality of first interconnects over said fifth insulating film.

14. (Currently amended) A manufacturing method of a semiconductor integrated circuit device according to claim 13, wherein each said first insulating film is an oxide film formed by thermal oxidation.

15. (Currently amended) A manufacturing method of a semiconductor integrated circuit device according to claim 13, wherein said third insulating film [[is]] portions are formed by CVD.

16. (Currently amended) A manufacturing method of a

semiconductor integrated circuit device according to claim 13, wherein an etching rate of said third insulating film portions is greater than that of said first insulating film portions.

17. (Currently amended) A manufacturing method of a semiconductor integrated circuit device according to claim 13, further comprising, between said step (d) and said step (e), heat treating said third insulating film portions.

18. (original) A manufacturing method of a semiconductor integrated circuit device according to claim 17, wherein said heat treatment is conducted at 900°C or greater.

19. (original) A manufacturing method of a semiconductor integrated circuit device according to claim 17, wherein said heat treatment is conducted at 1000°C or greater.

20. (Currently amended) A manufacturing method of a semiconductor integrated circuit device according to claim 13, wherein said third insulating film [[is]] portions are

thicker than said second insulating film portions.

21. (original) A manufacturing method of a semiconductor integrated circuit device according to claim 13, wherein said first and second conductive films are each made of polysilicon.

22. (withdrawn) A manufacturing method of a semiconductor integrated circuit device according to claim 13, wherein said first insulating film forming step comprises forming a groove in said semiconductor substrate and forming an oxide film in said groove.

23. (Currently amended) A manufacturing method of a semiconductor integrated circuit device according to claim 13, wherein the first insulating film portions in said first region [[is]] are narrower than the first insulating film portions in said second region.

24. (Currently amended) A manufacturing method of a semiconductor integrated circuit device having, in a first region of a semiconductor substrate, a plurality of first MISFETs each equipped with a gate electrode and source

drain regions and, in a second region of said semiconductor substrate, a plurality of second MISFETs each equipped with a gate electrode and source drain regions, comprising the steps of:

(a) forming a plurality of first insulating film portions in each of ~~between two adjacent regions of said~~ first MISFET forming regions in said first region and said second MISFET forming regions in said second region,

(b) introducing impurities in said second region, thereby forming ~~a first semiconductor region in said first region and a~~ second first semiconductor region regions as portions of the source and drain regions of said second MISFETs in said second region,

(c) forming a plurality of second insulating film ~~on~~ portions over a surface of said semiconductor substrate between said first insulating ~~films~~ film portions,

(d) depositing [[a]] third insulating film portions over at least said second insulating film portions and said first insulating film portions,

(e) removing said second and third insulating ~~films~~ film portions in said first region, and removing a portion of ~~the~~ said second and third insulating ~~films~~ film portions over a said ~~second~~ first semiconductor region in said

second region, ~~thereby forming a first opening,~~

(f) forming [[a]] first conductive film portions to be a provide gate ~~electrode~~ electrodes of said second MISFET MISFETs over said third insulating film portions between said first insulating film portions in said second region ~~of said semiconductor substrate,~~

(g) forming [[a]] fourth insulating film portions over the surface of the semiconductor substrate in said first region,

(h) forming [[a]] second conductive film portions to provide ~~to be a gate electrode~~ electrodes of said first MISFET MISFETs over said fourth insulating film portions in said first region, and

~~(i) introducing an impurity on the surface of said semiconductor substrate in order to form third semiconductor regions having a conductivity type contrary to that of said first semiconductor regions on both sides of said gate electrode of said first region and a fourth semiconductor region having the same conductivity type as that of said second semiconductor regions below said first opening in said second region~~

(i) introducing an impurity on the surface of said semiconductor substrate in order to form second

semiconductor regions as portions of the source and drain regions of said first MISFETs in said first region and to form third semiconductor regions as portions of the source and drain regions of said second MISFETs in said second region,

wherein each said first semiconductor region is formed deeper than said first insulating film portions in said second region, and

wherein each said third semiconductor region is surrounded by a corresponding one of said first semiconductor regions.

Claims 25-26 (cancelled)

27. (Currently amended) A manufacturing method of a semiconductor integrated circuit device according to claim 24, wherein the first insulating film portions in said first region [[is]] are narrower than the first insulating film portions in said second region.

28. (withdrawn) A manufacturing method of a semiconductor integrated circuit device having a first MISFET in a first region of a semiconductor substrate and a

second MISFET in a second region, comprising the steps of:

(a) forming a first insulating film in said first and second regions,

(b) depositing a first conductive film over said first insulating film in said first and second regions,

(c) removing the first insulating film and the first conductive film in said first region,

(d) forming a second insulating film in said first region over said semiconductor substrate,

(e) depositing a second conductive film in said first and second regions, and

(f) implanting an impurity to said first and second regions downward from a position above said second conductive film at an energy permitting the impurity to reach the substrate in said first region.

29. (withdrawn) A manufacturing method of a semiconductor integrated circuit device according to claim 28, further comprising the steps of:

(g) depositing a third conductive film over the second conductive film in each of said first and second regions, and

(h) removing a portion of said second and third

conductive films in said first region, forming a gate electrode of said first MISFET comprised of the second and third conductive films and removing said second and third conductive films from said second region.

30. (withdrawn) A manufacturing method of a semiconductor integrated circuit device according to claim 28, further comprising the steps of:

(g) depositing a third conductive film over the second conductive film in each of said first and second regions,

(h) removing a portion of said second and third conductive films in said first region, forming a gate electrode of said first MISFET comprised of the second and third conductive films and removing the second and third conductive films from said second region, and

(i) removing a portion of said first conductive film from said second region and forming a gate electrode of said second MISFET.

31. (withdrawn) A manufacturing method of a semiconductor integrated circuit device according to claim 28, which further comprising the step of:

(g) forming a fourth conductive film over said

semiconductor substrate within said first region.

32. (withdrawn) A manufacturing method of a semiconductor integrated circuit device according to claim 28, wherein implantation of the impurity stops at said first conductive film and the impurity does not reach said first insulating film.

33. (withdrawn) A manufacturing method of a semiconductor integrated circuit device according to claim 28, wherein implantation of the impurity stops at said first conductive film and the impurity does not reach said semiconductor substrate in said second region.

34. (withdrawn) A manufacturing method of a semiconductor integrated circuit device according to claim 28, wherein said first conductive film is thicker than said second conductive film.

35. (withdrawn) A manufacturing method of a semiconductor integrated circuit device according to claim 28, further comprising, between the step (d) and the step (e), heating in a nitrogen-containing atmosphere.

36. (withdrawn) A manufacturing method of a semiconductor integrated circuit device having a plurality of first MISFETs in a first region of a semiconductor substrate and a plurality of second MISFETs in a second region, comprising the steps of:

(a) forming a first insulating film between two adjacent regions of said first MISFET forming regions in said first region and said second MISFET forming regions in said second regions,

(b) forming a second insulating film over a surface of said semiconductor substrate between said first insulating films,

(c) depositing a third insulating film over said second insulating film in each of said first and second regions,

(d) removing said third insulating film from said first region,

(e) forming a first conductive film in said second region,

(f) exposing the surface of the semiconductor substrate in said first region while covering said third insulating film in said second region with said first

conductive film and forming a fourth insulating film, and

(g) forming a second conductive film over the fourth insulating film in said first region.

37. (withdrawn) A manufacturing method of a semiconductor integrated circuit device according to claim 36 further having a third region, comprising the steps of:

(a) forming the first insulating film in said third region,

(b) forming the first conductive film over said first insulating film in said third region,

(c) forming a fifth insulating film over said first conductive film in said third region, and

(d) forming the second conductive film over the fifth insulating film in said third region.

38. (withdrawn) A manufacturing method of a semiconductor integrated circuit device according to claim 37, wherein said first and second conductive films and said fifth insulating film constitute a capacitative element.

39. (withdrawn) A manufacturing method of a semiconductor integrated circuit device according to claim 36, wherein the first insulating film in said first region is narrower than the first insulating film in said second region.

Claims 40-58 (cancelled)

59. (Currently amended) A manufacturing method of a semiconductor integrated circuit device having a plurality of first MISFETs in a first region of a semiconductor substrate and a plurality of second MISFETs in a second region of said semiconductor substrate, comprising the steps of:

(a) forming a plurality of first insulating film portions over a surface of the semiconductor substrate in said first and second regions and a boundary region between said first and second regions,

(b) forming a plurality of second insulating film portions between said first insulating film portions over said surface of the semiconductor substrate,

[[(b)]] (c) depositing a ~~second~~ third insulating film over said first and second insulating film portions ~~film in said first and second regions~~,

(d) patterning said third insulating film in order to retain portions of said third insulating film in said boundary region and said second region,

[[(c)]] (e) forming a first conductive film portion

over said second third insulating film portion in said second region,

~~(d) exposing the surface of the semiconductor substrate in said first region while covering said second insulating film in said second region with said first conductive film, and forming a third insulating film, and~~

(f) forming a fourth insulating film portion over a surface of said semiconductor substrate in said first region,

[[(e)]] (g) forming a second conductive film portion over the ~~third~~ fourth insulating film portion in said first region,

(h) forming a fifth insulating film over said first, second and boundary regions, and

(i) forming a plurality of third conductive film portions over said fifth insulating film.

60. (Currently amended) A manufacturing method of a semiconductor integrated circuit device having a plurality of first MISFETs in a first region of a semiconductor substrate and a plurality of second MISFETs in a second region of said semiconductor substrate, comprising the steps of:

(a) forming a plurality of first insulating film portions made of [[a]] thermally oxidized film on a surface of the semiconductor substrate in said first and second regions and a boundary region between said first and second regions,

(b) selectively introducing impurities into said semiconductor substrate, thereby forming first impurity regions in said second region,

(c) forming a plurality of second insulating film portions between said first insulating film portions over said surface of the semiconductor substrate,

[[(b)]] (d) depositing a ~~second~~ third insulating film over said first and second insulating films ~~film in said first and second regions~~,

(e) patterning said third insulating film in order to retain portions of said third insulating film in said boundary region and said second region,

[[(c)]] (f) forming a first conductive film portion over said ~~second~~ third insulating film in said second region,

~~(d) exposing the surface of the semiconductor substrate in said first region while covering said second insulating film in said second region with said first~~

~~conductive film, and forming a third insulating film made of a thermally oxidized film, and~~

(g) forming a fourth insulating film portion over a surface of said semiconductor substrate in said first region,

[[(e)]] (h) forming a second conductive film portion over the third fourth insulating film portion in said first region,

(i) introducing impurities into said semiconductor substrate, thereby forming second impurity regions,

(j) forming a fifth insulating film over said first, second and boundary regions, and

(k) forming a third conductive film portion over said fifth insulating film,

wherein a portion of said third conductive film portion in said boundary region is formed over a first insulating film portion via portions of said third and fifth insulating films,

wherein said first impurity regions and second impurity regions formed in said second region compose source and drain regions of said plurality of second MISFETs,

wherein each said first impurity region in said second region surrounds a corresponding second impurity region, and

wherein each said first impurity region in said second region surrounds at least one corresponding first insulating film portion.

Please add the following claims:

61. (New) A manufacturing method of a semiconductor integrated circuit device having a plurality of MISFETs in a semiconductor substrate, comprising the steps of:

(a) forming a plurality of first insulating film portions on a surface of said semiconductor substrate,

(b) forming a plurality of second insulating film portions between said first insulating film portions over the surface of said semiconductor substrate,

(c) forming a plurality of third insulating film portions over said plurality of first insulating film portions and said second insulating film portions,

(d) forming a plurality of first conductive film portions to serve as gate electrodes of said plurality of MISFETs over said third insulating film portions,

(e) forming a fourth insulating film in order to cover said plurality of MISFETs, and

(f) forming a second conductive film over said fourth insulating film,

wherein at least a portion of said second conductive film is formed over a first insulating film portion via a third insulating film portion and a portion of said fourth insulating film.

62. (New) A manufacturing method of a semiconductor integrated circuit device having a plurality of MISFETs in a semiconductor substrate, comprising the steps of:

(a) forming a plurality of first insulating film portions on a surface of said semiconductor substrate,

(b) selectively introducing impurities into said semiconductor substrate, thereby forming first impurity regions,

(c) forming a plurality of second insulating film portions between said first insulating film portions over the surface of said semiconductor substrate,

(d) forming a plurality third insulating film portions over said first and second insulating film portions,

(e) forming a plurality of first conductive film portions to serve as gate electrodes of said plurality of MISFETs over said third insulating film portions, and

(f) introducing impurities into said semiconductor substrate, thereby forming second impurity regions,

wherein said first impurity regions and second impurity regions compose portions of source and drain regions of said plurality of MISFETs,

wherein each said first impurity region surrounds a corresponding second impurity region, and

wherein each said first impurity region surrounds at least one corresponding first insulating film portion.

63. (New) A manufacturing method of a semiconductor integrated circuit device according to claim 24, wherein the impurity concentration of said first semiconductor regions is lower than that of said third semiconductor regions.

64. (New) A manufacturing method of a semiconductor integrated circuit device according to claim 59, wherein said third insulating film is formed by a CVD method.

65. (New) A manufacturing method of a semiconductor integrated circuit device according to claim 60, wherein said third insulating film is formed by a CVD method.

66. (New) A manufacturing method of a semiconductor integrated circuit device according to claim 60, wherein the impurity concentration of said first impurity regions is lower than that of said second impurity regions.

67. (New) A manufacturing method of a semiconductor integrated circuit device according to claim 60, wherein said first insulating film portions formed in said second region are narrower than a first insulating film portion formed in said boundary region.

68. (New) A manufacturing method of a semiconductor integrated circuit device according to claim 61, wherein said third insulating film is formed by a CVD method.

69. (New) A manufacturing method of a semiconductor integrated circuit device according to claim 62, wherein said third insulating film portions are formed by a CVD method.

70. (New) A manufacturing method of a semiconductor integrated circuit device according to claim 62, wherein the impurity concentration of said first impurity regions is lower than that of said second impurity regions.

71. (New) A manufacturing method of a semiconductor integrated circuit device according to claim 1, wherein at least one of said plurality of first interconnects is formed over a first insulating film portion via a third insulating film portion and a portion of said fifth insulating film.

72. (New) A manufacturing method of a semiconductor integrated circuit device according to claim 13, wherein at least one of said plurality of first interconnects is formed over a first insulating film portion via a third insulating film portion and a portion of said fifth insulating film.

73. (New) A manufacturing method of a semiconductor integrated circuit device according to claim 59, wherein at least one of said third conductive film portions is formed

over a first insulating film portion via portions of said third and fifth insulating films.